DECLARATION

I, Akira Yamada, a citizen of Japan, residing at 3490-78 Nagara, Gifu-shi, Gifu-ken, Japan, hereby declare that I am the translator of the attached document and certify that, to the best of my knowledge and belief, it is a true and accurate translation of Japanese Patent Application No. 2000-362252, filed on November 29, 2000.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true,

Akira Yamada
Translator
Dated this 13th date of October, 2005

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[Title Of the Document] Specification

[Title of the Invention] ELECTRONIC TUNING SYSTEM

[Scope of Claims]

[Claim 1] An electronic tuning system including an electronic tuner for tuning a local frequency signal to radio waves on an arbitrary channel, the electronic tuning system comprising:

a voltage controlled oscillator for varying the frequency of the local frequency signal based on a predetermined control voltage;

a booster circuit for boosting a source voltage to generate a boosted voltage in order to ensure the control voltage of the voltage controlled oscillator; and

a non-volatile memory for storing channel selection information, which is the tuning information of the voltage controlled oscillator, wherein the boosted voltage of the booster circuit is utilized as write voltage of the channel selection information for the non-volatile memory.

[Claim 2] The electronic tuning system according to claim 1, wherein the electronic tuner includes:

a program frequency divider for dividing the local frequency signal oscillated by the voltage controlled oscillator in accordance with a programmably designated frequency division ratio;

a phase comparator for comparing the frequency and phase of the divided signal with the frequency and phase of a signal oscillated by a reference oscillator to output an average DC voltage proportional to the differences; and

a low-pass filter for low-band filtering the average DC voltage signal, wherein the control voltage of the voltage controlled oscillator is the sum of the output voltage of the low-pass filter and the boosted voltage of the booster circuit, and the channel selection information is stored in

the non-volatile memory as information indicating the frequency division ratio when tuning is completed that is designated by the program frequency divider.

[Claim 3] The electronic tuning system according to claim 1 or 2, wherein the booster circuit includes:

a coil coupled to a battery;

a switching element for periodically grounding DC current supplied to the coil;

a zener diode for clamping an electromotive force induced in the coil in accordance with a change in the current to a predetermined voltage; and

a capacitor for smoothing the voltage clamped by the zener diode.

[Claim 4] The electronic tuning system according to any one of claims 1 to 3, further comprising:

a voltage application control means for monitoring generation of a write request of the channel selection information to the non-volatile memory and applying the boosted voltage of the booster circuit to the non-volatile memory only when the write request is generated.

[Claim 5] The electronic tuning system according to any one of claims 1 to 4, wherein the non-volatile memory is a flash memory for generating erasure voltage and write voltage based on the boosted voltage of the booster circuit.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to an electronic tuning system, and more particularly, to an electronic tuning system which comprises an electronic tuner for tuning to radio waves on a broadcast channel of television broadcasting, radio broadcasting and the like, or a local channel used in a variety of radio devices.

[0002]

[Prior Art]

As is well known, in the television broadcasting and radio broadcasting, respective broadcasting stations are assigned radio waves in different frequency bands from one another as broadcast channels. Thus, on the receiver side, radio waves on a desired broadcast channel are selectively received to enjoy contents of broadcasting provided by a desired broadcasting station.

[0003]

Generally, a receiver for receiving radio waves on a particular channel is configured in the following manner. A received signal received through an antenna is mixed with a local frequency signal supplied from a local oscillator by a mixer. A signal generated from the sum or the difference of the two signals by a mixer is supplied to an intermediate frequency filter. The intermediate frequency filter selectively supplies a detector circuit only with a signal having an intermediate frequency. The detector circuit demodulates the received signal corresponding to a predetermined broadcast channel.

[0004]

The receiver comprises an electronic tuner for selecting a desired broadcast channel. The electronic tuner adjusts (tunes) a frequency band of the local frequency signal supplied from the local oscillator such that only the received signal on the desired broadcast channel passes through the intermediate frequency filter. The electronic tuner has a voltage controlled oscillator (VCO) including a local oscillator, and controls a voltage applied to the voltage controlled oscillator to control the frequency band of the local frequency signal output from the oscillator.

[0005]

In an electronic tuning system comprising an electronic tuner, channel selection information on a broadcast channel selected through a voltage controlled oscillator (frequency information or tuning control information) is stored in a memory, such that the channel selection information stored in the memory is read upon next channel selection to permit prompt tuning to the broadcast channel. For this reason, the channel selection (tuning control) and writing the channel selection information into the memory have been previously performed for a plurality of broadcast channels, so that the selection of an arbitrary broadcast channel can be instantaneously made through an extremely simple operation of reading such channel selection information from the memory.

[0006]

[Problems that the Invention is to Solve]

Memories used in such electronic tuning systems often require a sustain current for a RAM (Random Access Memory) or the like. Therefore, when such an electronic tuning system is equipped in a portable device driven by a battery such as a dry battery, the following disadvantages will result.

[0007]

Specifically, a device which employs a dry battery as a power source such as a portable device essentially involves replacement of dry batteries when the device is used for a long time. However, the replacement of batteries results in interruption of the sustain current, so that information stored in a memory is erased. In such a situation, after the replacement of batteries, the user is forced to perform complicated operations which involves selecting (tuning) each broadcast channel and writing the channel selection information into the memory.

[0008]

Accordingly, it is an object of the present invention to

provide an electronic tuning system which prevents erasure of information on channels selected through electronic tuning.

[0009]

[Means for Solving the Problems]

The gist of the invention of claim 1 is an electronic tuning system including an electronic tuner for tuning a local frequency signal to radio waves on an arbitrary channel, the electronic tuning system comprising a voltage controlled oscillator for varying the frequency of the local frequency signal based on a predetermined control voltage, a booster circuit for boosting a source voltage to generate a boosted voltage in order to ensure the control voltage of the voltage controlled oscillator, and a non-volatile memory for storing channel selection information, which is the tuning information of the voltage controlled oscillator, wherein the boosted voltage of the booster circuit is utilized as write voltage of the channel selection information for the non-volatile memory.

[0010]

With the above configuration, by storing channel selection information, which is tuning information of the voltage controlled oscillator, the channel selection information may be held regardless of whether or not there is hold current. Further, with the above configuration, the control voltage of the voltage controlled oscillator and the write voltage of the channel selection information for the non-volatile memory is ensured by the single booster circuit that boosts the source voltage. This enhances the miniaturization of the electronic tuning system.

[0011]

The gist of the invention of claim 2 is in that in the invention of claim 1, the electronic tuner includes a program frequency divider for dividing the local frequency signal

oscillated by the voltage controlled oscillator in accordance with a programmably designated frequency division ratio, a phase comparator for comparing the frequency and phase of the divided signal with the frequency and phase of a signal oscillated by a reference oscillator to output an average DC voltage proportional to the differences, and a low-pass filter for low-band filtering the average DC voltage signal, wherein the control voltage of the voltage controlled oscillator is the sum of the output voltage of the low-pass filter and the boosted voltage of the booster circuit, and the channel selection information is stored in the non-volatile memory as information indicating the frequency division ratio when tuning is completed that is designated by the program frequency divider.

[0012]

With the above configuration, the local frequency signal oscillated by the voltage controlled oscillator is accurately stabilized at a predetermined value.

The gist of the invention of claim 3 is in that in the invention of claim 1 or 2, the booster circuit includes a coil coupled to a battery, a switching element for periodically grounding DC current supplied to the coil, a zener diode for clamping an electromotive force induced in the coil in accordance with a change in the current to a predetermined voltage, and a capacitor for smoothing the voltage clamped by the zener diode.

[0013]

With the above configuration, the boosting operation is performed with high efficiency through an extremely simple configuration.

The gist of the invention of claim 4 is in that in the invention of any one of any one of claims 1 to 3, the electronic tuning system further comprises a voltage

application control means for monitoring generation of a write request of the channel selection information to the non-volatile memory and applying the boosted voltage of the booster circuit to the non-volatile memory only when the write request is generated.

[0014]

With the above configuration, the voltage application controller monitors the generation of a write request of the channel selection information to the non-volatile memory and applies the boosted voltage of the booster circuit to the non-volatile memory only when the write request is generated. Thus, the stress applied to the non-volatile memory is lowered compared to when high voltage is constantly applied.

[0015]

The gist of the invention of claim 5 is in that in the invention of any one of any one of claims 1 to 4, the non-volatile memory is preferably a flash memory for generating erasure voltage and write voltage based on the boosted voltage of the booster circuit.

[0016]

[Embodiments of the Invention]

In the following, a portable radio receiver according to a first embodiment of the present invention will be described with reference to the drawings. An electronic tuning system of the present invention is applied to the portable radio receiver.

[0017]

Fig. 1 is a block diagram showing the entire structure if the radio receiver.

As illustrated in Fig. 1, the radio receiver converts a received signal into an intermediate frequency signal having a predetermined intermediate frequency, demodulates the intermediate frequency signal, and retrieves an audio signal

from radio waves on a desired broadcast channel. The radio receiver comprises an antenna 10; a mixer 11 for mixing a received signal received by the antenna 10 with a local oscillating frequency signal supplied from a local oscillator 20; an intermediate frequency filter 12 which passes therethrough only an intermediate frequency signal from the mixed frequency signal output from the mixer 11; a detector circuit 13 for demodulating the intermediate frequency signal supplied from the intermediate frequency filter 12 to an audio signal; and a speaker 14 (audio circuit) for outputting sound in accordance with the audio signal demodulated by the detector circuit 13.

[0018]

Next described will be a sequence of operations from the demodulation of the received signal received by the antenna 10 to delivery of sound from the speaker 14.

First, the mixer 11 subtracts the frequency of the received signal received by the antenna 10 from the frequency of the local frequency signal oscillated from the local oscillator 20 to generate a mixed frequency signal having the frequency resulting from the subtraction. The intermediate frequency filter 12 supplies the detector circuit 13 only with a signal in a predetermined intermediate frequency band from among the mixed frequency signal.

[0019]

The detector circuit 13 demodulates the intermediate frequency signal to generate an audio signal irrespective of the frequency band of a broadcast channel to be selected. The speaker 14 outputs sound in accordance with the audio signal. The detector circuit 13 also generates information indicating whether the intermediate frequency signal includes an audio signal from an arbitrary broadcasting station.

[0020]

The frequency of the local frequency signal oscillated from the local oscillator 20 is set by adding the intermediate frequency to the frequency of a desired broadcast channel, so that only a signal at the frequency of the desired broadcast channel is selectively demodulated. For changing a broadcast channel, the frequency band of the local frequency signal output from the local oscillator 20 is also changed (tuned). This change results in a change in signal components of the received signal received by the antenna 10 which pass through the intermediate frequency filter 12, so that an audio signal corresponding to the changed broadcast channel is demodulated in the detector circuit 13.

[0021]

The frequency of the local oscillating signal output from the local oscillator 20 is changed by changing the resonant frequency of the local oscillator 20 in accordance with the capacitance of a varactor diode 21 coupled between the local oscillator 20 and a ground. The capacitance of the varactor diode 21 is changed in accordance with a voltage applied to a cathode of the varactor diode 21. Specifically, in this embodiment, a voltage controlled oscillator is formed by the local oscillator 20 and the varactor diode 21. Then, the foregoing tuning operation is implemented by controlling the oscillating frequency of the voltage controlled oscillator.

[0022]

Next, the tuning operation will be described.

In this embodiment, a PLL (Phase Locked Loop) method is employed as a tuning method for tuning the local frequency of the local oscillator 20 to the sum of a desired frequency and the intermediate frequency. Specifically, the local frequency of the local oscillator 20 is divided in a ratio of

the sum of the desired frequency and the intermediate frequency to a reference frequency to generate a divided frequency signal, and the voltage controlled oscillator is feedback controlled such that the frequency of the divided frequency signal matches the reference frequency.

[0023]

Specifically, a direct current (DC) component of the local frequency signal output from the local oscillator 20 is cut by a DC cut capacitor 22, and the local frequency signal deprived of the DC component is amplified by a parallel circuit comprised of an inverter 23 and a resistor 24.

[0024]

A programmable frequency divider 25 divides the amplified local frequency signal by a predetermined division ratio to generate a divided local frequency signal. The predetermined division ratio is calculated by dividing the sum of the desired frequency and the intermediate frequency by the reference frequency. A phase comparator 26 compares the phase and frequency of the divided local frequency signal with the phase and frequency of the reference frequency signal output from a reference oscillator 27.

[0025]

The phase comparator 26 generates an average DC voltage signal which is proportional to the phase difference and the frequency difference. A low-pass filter 28 removes an alternating current (AC) component of the average DC voltage signal to generate a filtered average DC voltage signal. The filtered average DC voltage signal is applied to the cathode of the varactor diode 21.

[0026]

A boosted voltage (for example, "15 V") from a booster circuit 30 is added to the voltage of the filtered average DC voltage signal from the low-pass filter 28. In other words,

the cathode of the varactor diode 21 is applied with a voltage which varies in a range of "zero to the boosted voltage" in accordance with the output voltage of the low-pass filter 28.

[0027]

When the varactor diode 21 is applied with a voltage which varies in accordance with the phase difference and the frequency difference in the foregoing manner, the frequency of the local frequency signal output from the local oscillator 20 also changes in accordance with the phase difference and frequency difference. Eventually, a feedback control is conducted to reduce the phase difference and frequency difference to "0." In this way, the frequency of the frequency signal output from the local oscillator 20 is locked to the frequency generated by adding the intermediate frequency to the desired frequency.

[0028]

Next, the booster circuit 30 will be described.

As illustrated in Fig. 1, the booster circuit 30 is preferably a DC-DC converter which makes use of inductive electromotive force of a coil for boosting. Specifically, a counter electromotive force is generated by suddenly changing a current flowing from a battery (dry battery) 31, for example, having a source voltage of "1.5 V" to a coil 32. This counter-electromotive force is clamped to a predetermined voltage equal to or higher than the source voltage, and the clamped voltage is smoothed by a capacitor 34.

[0029]

Here, the current flowing through the coil 32 is suddenly changed by periodically turning ON/OFF a transistor 35, which serves as a switching element, to periodically conduct the DC current flowing through the coil 32 to the

ground. Specifically, the transistor 35 has a source terminal coupled to a node between the coil 32 and a zener diode 33, and a drain terminal of the transistor 35 is grounded. A pulse signal is applied to a gate terminal of the transistor 35 from a pulse generator 36 to synchronously conduct the current flowing through the coil 32 to the ground to cause a sudden change in the current through the coil 32.

[0030]

For clamping the electromotive force induced in the coil 32 by such a change in current, the zener diode 33 having a breakdown voltage set, for example, at "15 V" is used. The voltage clamped by the zener diode 33 is smoothed by the capacitor 34. In this case, a boosted output (boosted voltage) by the booster circuit 30 is "15 V" corresponding to the breakdown voltage of the zener diode 33. This boosted voltage is added to the output voltage of the low-pass filter 28.

[0031]

Next, description will be made on automatic broadcast channel tuning performed in the receiver of Fig. 1 by the electronic tuner including the mixer 11, the intermediate frequency filter 12, the detector circuit 13, and the PLL as described above.

[0032]

When a broadcast channel search instruction is supplied to a microcomputer 50 through a manipulation on a manipulation unit 40 by the operator, the microcomputer 50 gradually changes the frequency division ratio for the programmable frequency divider 25. Specifically, the microcomputer 50 is supplied with a signal DM indicating whether a received signal on a broadcast channel has been supplied from the detector circuit 13, and the microcomputer 50 changes the frequency division ratio for the programmable

frequency divider 25 based on the signal DM until a received signal on the broadcast channel is received.

[0033]

When the microcomputer 50 receives the signal DM indicating that a received signal on a broadcast channel is supplied from the detector circuit 13, the microcomputer 50 displays on a display (not shown) that a particular broadcast channel has been received, for example, through the manipulation unit 40. When the microcomputer 50 is supplied with a broadcast channel store instruction from the manipulation unit 40 through a manipulation on the manipulation unit 40 by the operator, the microcomputer 50 stores the value of the frequency division ratio currently supplied to the programmable frequency divider 25 in a flash memory 100 as broadcast channel selection information. Subsequently, when this broadcast channel is selected through a manipulation on the manipulation unit 40 by the operator, the microcomputer 50 reads the value of the frequency division ratio (channel selection information) corresponding to the selected broadcast channel, and supplies the read value of the frequency division ratio to the programmable frequency divider 25. Thus, the broadcast channel is tuned promptly. Likewise, for other broadcast channels, channel selection information (frequency division ratio) is stored in the flash memory 100, and the selection information (frequency division ratio) is read from the flash memory 100.

[0034]

The flash memory 100, which is an electrically erasable and programmable read only memory (EEPROM), stores the channel selection information. Therefore, even if the power to the memory 100 is interrupted due to replacement of the battery (dry battery) 31, the selection information stored in the memory 100 is not erased but held therein.

[0035]

For erasing data in the flash memory 100 or writing data thereinto, a high voltage of approximately 12 to 15 V is required. In this embodiment, the boosted voltage from the booster circuit 30 is utilized as a data erasing voltage or a data writing voltage.

[0036]

Next, the configuration of the flash memory 100 will be described with reference to Fig. 2.

The flash memory 100 comprises a memory array 110 in which a plurality of memory cells are arranged in rows and columns. Word lines and source lines associated with the respective memory cells are coupled to a row decoder 111, and bit lines associated with respective memory cells are coupled to a column decoder 112.

[0037]

The row decoder 111 applies the source lines with a high voltage (for example, "12 V") for writing, and applies the word lines with a high voltage (for example, "15 V") for erasure. A voltage converter circuit 130 receives the boosted voltage from the booster circuit 30 to generate the high voltage supplied to the row decoder 111.

[0038]

The column decoder 112 reads data from a memory cell through a bit line, and writes data held by an input/output buffer 122 into a memory cell.

[0039]

An address buffer 121 once holds address data for a memory cell specified by the microcomputer 50, and supplies the address data to the row decoder 111 and the column decoder 112 at a predetermined timing specified by a control unit 120.

[0040]

Now, description will be made on a read, a write and an erase mode of the flash memory 100.

In the read mode, the address buffer 121 is supplied with address data Add, from the microcomputer 50, indicative of the location of a memory cell from which data is to be read, and the control unit 120 is supplied with a read instruction Read. Then, the address buffer 121 once holds the address data of the specified memory cell, and supplies the row decoder 111 and the column decoder 112 with the address data at a predetermined timing specified by the control unit 120. The row decoder 111 activates a word line of a predetermined row in accordance with the address data. The column decoder 112 supplies the input/output buffer 122 with data on a bit line of a predetermined column in accordance with the address data. The data supplied to the input/output buffer 122 in this way is captured into the microcomputer 50 through a data bus (I/O).

[0041]

In the write mode, the address buffer 121 is supplied with address data Add, from the microcomputer 50, indicative of the location of a memory cell into which data is to be written, the input/output buffer 122 is supplied with write data through the data bus (I/O), and the control unit 120 is supplied with a write instruction Write. Then, the address buffer 121 once holds the address data of the specified memory cell, and supplies the row decoder 111 and the column decoder 121 with the address data at a predetermined timing specified by the control unit 120. The voltage converter circuit 130 step-downs the output voltage of the booster circuit 30 to "12 V" in response to an instruction from the control unit 120, and supplies the step-down voltage to the row decoder 111. The row decoder 111 applies a source line coupled to the specified memory cell with the step-down

voltage supplied from the voltage converter circuit 130. The column decoder 112 applies a bit line coupled to the specified memory cell with a voltage corresponding to write data. In this way, the data is written into the predetermined memory cell.

[0042]

In the erase mode, the address buffer 121 is supplied with address data Add, from the microcomputer 50, indicative of the location of a memory cell from which data is to be erased, and the control unit 120 is supplied with an erase instruction Erase. The address buffer 121 once holds the address data of the specified memory cell, and supplies the row decoder 111 with the address data at a predetermined timing specified by the control unit 120. The voltage converter circuit 130 supplies the row decoder 111 with the output voltage "15 V" of the booster circuit 30 in response to an instruction from the control unit 120. The row decoder 111 applies a word line of an associated row address with the high voltage supplied from the voltage converter circuit 130. This results in collective erasure of information stored in memory cells corresponding to the associated row address.

[0043]

In the foregoing manner, in this embodiment, the high voltage generated by the booster circuit 30 for electronic tuning is also used for writing data into and erasing data from the flash memory 100. This eliminates the need for providing a booster circuit such as a charge pump circuit on a semiconductor substrate, on which the flash memory 100 is fabricated, for generating a high voltage for use in writing and erasure, resulting in a reduction in the size of the flash memory 100.

[0044]

The radio receiver according to the first embodiment

provides the following advantages.

(1) Since channel selection information is held by use of the flash memory 100 even if the supplied current is interrupted, the channel selection information is prevented from erasure. Also, since the high voltage for writing data into or erasing data from the flash memory 100 is generated from the boosted voltage generated by the booster circuit 30 used for ensuring a control voltage for the voltage controlled oscillator, a reduction in the size of the electronic tuning system is promoted.

[0045]

(2) Since a DC-DC converter is used for the booster circuit 30, a highly efficient boosting operation can be implemented in an extremely simple configuration.

(Second Embodiment)

In the following, a portable radio receiver according to a second embodiment of the present invention will be described with reference to Fig. 3, centered on differences with the first embodiment. Elements shown in Fig. 3 that are like to those shown in Fig. 2 are denoted with the same reference numerals.

[0046]

In the first embodiment, in order for the output voltage of the booster circuit 30 utilizing the drive of the voltage controlled oscillator to be used to ensure high voltage for writing or reading data with the flash memory 100, the voltage converter circuit 130 and the booster circuit 30 are connected in the aspects shown in Figs. 1 and 2. However, in such a configuration, the output voltage of the booster circuit 30 is constantly applied to the voltage converter circuit 130. This applies stress to the voltage converter circuit 130.

[0047]

Accordingly, in the second embodiment, a protection switch is coupled between the booster circuit 30 and the voltage converter circuit 130. The protection switch supplies the voltage converter circuit 130 with a boosted voltage in response to a write (or erase) request to a flash memory 200. Therefore, the protection switch relieves a stress applied on the voltage converter circuit 130.

[0048]

Fig. 3 is a block diagram showing the entire structure of the flash memory 200 of this embodiment having such functions. As shown in the drawing, when the flash memory 200 requires the boosted voltage from the booster circuit 30 in the write mode or the erase mode, the protection switch 210 supplies the voltage converter circuit 130 with the boosted voltage by conducting between the voltage converter circuit 130 and the booster circuit 30. The protection switch 210 is controlled by a control unit 220, such that a boosted voltage input terminal of the voltage converter circuit 130 is selectively coupled to the booster circuit 30 or the ground.

[0049]

Specifically, the protection switch 210 connects the output terminal of the booster circuit 30 to the input terminal of the voltage converter circuit 130 when the protection switch 210 receives a signal having a logical "H" level from the control unit 220. The protection switch 210 electrically disconnects the output terminal of the booster circuit 30 from the input terminal of the voltage converter circuit 130 to ground the input terminal of the voltage converter circuit 130 when the protection switch 210 receives a signal having a logical "L" level from the control unit 220. The protection switch 210 includes a p-channel transistor T1, an n-channel transistor T2, a p-channel transistors T3, an n-

channel transistor T4, and an inverter 211.

[0050]

In addition to advantages (1) and (2) of the first embodiment, the second embodiment provides the following advantages.

(3) The provision of the protection switch 120 relieves a stress applied to the voltage converter circuit 130 and hence a stress applied to the flash memory 200.

[0051]

The second embodiment may be modified in the following manner.

The protection switch 210 may be coupled external to the flash memory 200.

[0052]

In each of the above embodiments, the following elements may be modified.

Not limited to a DC-DC converter, another one, for example, a charge pump circuit may be used as the booster circuit.

[0053]

In place of the flash memory, arbitrary non-volatile memories may be used. In this event, for reducing the size and power consumption of the electronic tuning system having a non-volatile memory, a voltage for use in writing channel selection information into the non-volatile memory is preferably generated from the booster circuit for ensuring a control voltage for the voltage controlled oscillator.

[0054]

Not limited to the PLL, electronic tuning schemes may be employed such as a frequency synthesizer including a direct digital synthesizer, a voltage synthesizer, and the like.

[0055]

A booster circuit may be fabricated on a semiconductor

substrate of the non-volatile memory such that a control voltage for the voltage controlled oscillator is ensured from a boosted voltage of the booster circuit.

A mixed frequency signal of the mixer 11 may be generated by a method other than the subtraction of a frequency signal received by the antenna from the frequency signal oscillated by the local oscillator 20.

[0056]

The electronic tuning system of the present invention may be applied not only to radio receivers but also to television receivers and transceivers, by way of example.

[Brief Description of the Drawings]

[Fig. 1] Schematic block diagram of a portable radio receiver according to a first embodiment of the present invention.

[Fig. 2] Schematic block diagram of a flash memory of the radio receiver of Fig. 1.

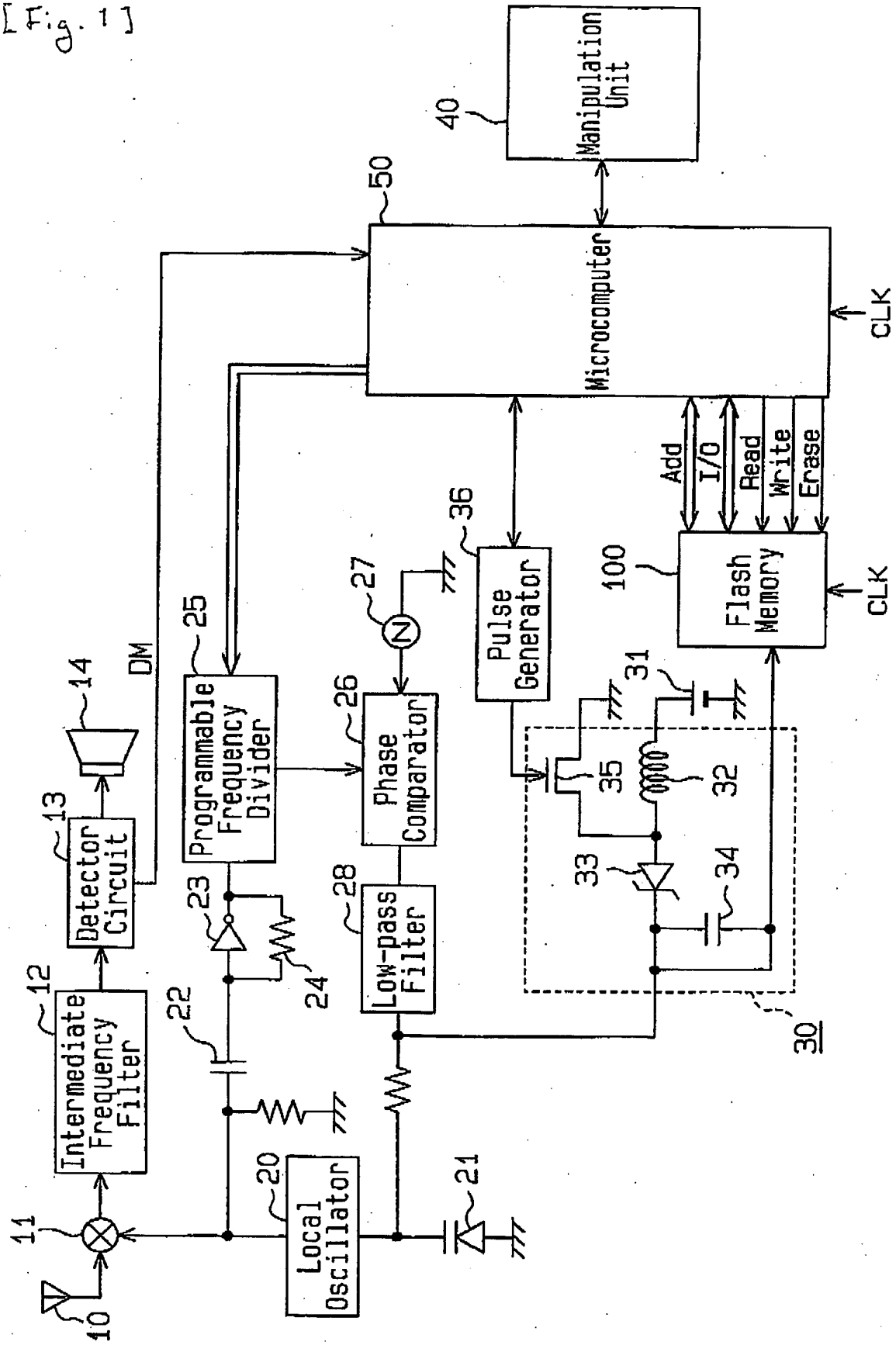
[Fig. 3] Schematic block diagram of a flash memory of a portable radio receiver according to a second embodiment of the present invention.

[Description of the Reference Numerals]

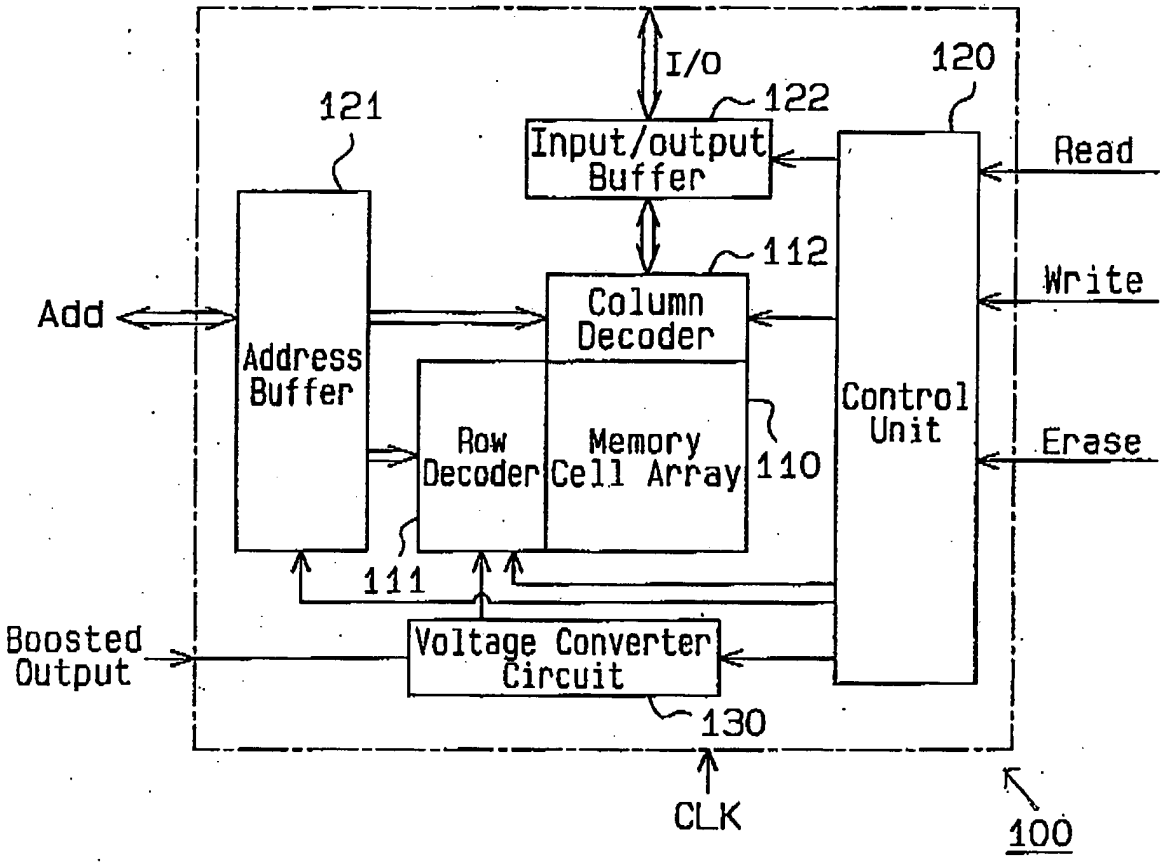
10...antenna, 11...mixer, 12...intermediate frequency filter, 13...detector circuit, 14...speaker, 20...local oscillator, 21...varactor diode, 22...DC cut capactitor, 23...inverter, 24...resistor, 25...program frequency divider, 26...phase comparator, 27...reference oscillator, 28...low-pass filter, 30...booster circuit, 31...system power source, 32...coil, 33...zener diode, 34...capacitor, 35...transistor, 36...pulse generator, 40...manipulation unit, 50...microcomputer, 100, 200...flash memory, 110...memory cell array, 111...row decoder, 112...column decoder, 120, 220...control unit, 121...address buffer, 122...input/output buffer, 130...voltage converter circuit, 210...protection switch, 211...inverter

[Title of the Document] Drawings

[Fig. 1]



[Fig. 2]


I/O
120
121
122
Input/output Buffer
Read
112
Write
Add
Column Decoder
Address Buffer
Control Unit
Row Decoder
Memory Cell Array
110
Erase
111
Boosted Output
Voltage Converter Circuit
130
CLK
100

[Title of the Invention] Abstract

[Abstract]

[Purpose] Providing an electronic tuning system enabling electronically tuned channel selection information to be semi-permanently held even when used for a portable device or the like.

[Means for Solving the Problems] A reception signal received by an antenna 10 and a local frequency signal oscillated by a local oscillator 20 are mixed by a mixer 11 to provide mixed frequency signals to an intermediate frequency filter 12. Among the mixed frequency signals, an intermediate frequency filter 12 selectively provides only signals of an intermediate frequency band to a detection circuit 13, in which the signals are demodulated. To select a broadcasted channel that is demodulated by the detection circuit 13, a local oscillator 20 voltage controls the oscillation frequency of a local oscillator 20. This control information, or channel section information, is stored in a flash memory 100. The output voltage of a booster circuit 30, which ensures the control voltage of a voltage controlled oscillator, is used as voltage for writing data to the flash memory 100.

[Selected Drawing] Fig. 1